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In this paper, we present a new integrated synthesis and partitioning method for multiple-FPGA applications. Our approach bridges the gap between HDL synthesis and physical partitioning by fully exploiting the design hierarchy. We propose a novel multiple-FPGA synthesis and partitioning method which is performed in three phases: (1) fine-grained synthesis, (2) functional-based clustering, and (3) hierarchical set-covering partitioning. This method first synthesizes a design specification in ...

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Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays February 2000

This paper presents a benchmark suite for evaluating a configurable computing system's infrastructure, both tools and architecture. A novel aspect of this work is the use of stressmarks, benchmarks that focus on a specific characteristic or property of interest. This is in contrast to traditional approaches that utilize functional benchmarks, benchmarks that emphasize measuring end-to-end execution time. This suite can be used to assess a broad range of con ...

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Wen-Jong Fang , Allen C.-H. Wu , Duan-Ping Chen
Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays February 1997

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Melvin A. Breuer , Alice C. Parker
Proceedings of the eighteenth design automation conference on Design automation June 1981
This paper presents a philosophical view of the changing field of design verification. The evolution of simulation and fault simulation are briefly summarized. Current research issues in design verification are discussed. The paper concludes with a discussion of the future direction simulation will take, along with other techniques destined to compete with simulation for the design verification task.

8 A finite machine description of a lexical analysis using table look-up 85%
D. Soda , G. W. Zobrist
Proceedings of the seventeenth annual ACM conference on Computer science : Computing trends in the 1990's: Computing trends in the 1990's February 1989
A lexical analysis is described using a finite state machine to express the top level of the algorithm. The lexical analyzer exploits table lookup to facilitate the determination of tokens. The table lookup procedure alleviates the process of developing a conplicated set of construction rules.

9 LIBRA—a library-independent framework for post-layout performance optimization 82%
Ric Chung-Yang Huang , Yucheng Wang , Kwang-Ting Chen
Proceedings of the 1998 international symposium on Physical design April 1998
In this paper we present a post-layout timing optimization framework which (1) is library-independent such that it can take the logic-optimized Verilog file as its input netlist, (2) provides a prototype interface which can communicate with any vendor's physical design tools to obtain the accurate timing, topological and physical information, and perform ECO placement and routing, and (3) has fast and powerful rewiring routines that offer an extra solution space beyond the existing physical ...

10 Architecture-level power estimation and design experiments 80%
Rita Yu Chen , Mary Jane Irwin , Raminder S. Bajwa
ACM Transactions on Design Automation of Electronic Systems (TODAES)

January 2001
Volume 6 Issue 1

Architecture-level power estimation has received more attention recently because of its efficiency. This article presents a technique used to do power analysis of processors at the architecture level. It provides cycle-by-cycle power consumption data of the architecture on the basis of the instruction/data flow stream. To characterize the power dissipation of control units, a novel hierarchical method has been developed. Using this technique, a power estimator is implemented for a commercia ...

11 A hierarchical functional structuring and partitioning approach for multiple-FPGA implementations 80%

Wen-Jong Fang , Allen C.-H. Wu
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997

In this paper, we present a new synthesis and partitioning approach for multiple-FPGA implementations from Register-Transfer-Level (RTL) netlists. Our approach bridges the gap between RTL/logic synthesis and physical partitioning by finely tuning logic implementations suited for multiple-FPGA systems. We propose a hierarchical functional structuring and partitioning method which fully exploits the design structural hierarchy by decomposing RTL components into sets of logic sub-functions. This al ...

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John Paul Shen
Proceedings of 1986 fall joint computer conference on Fall joint computer conference November 1999

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Yuan Xie , Wayne Wolf , Haris Lekatsas
Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture December 2001

In embedded system design, memory has been one of the most restricted resources. Reducing program size has been an important goal when designing an embedded system. Most of the previous work on code compression has targeted RISC architectures. Recently VLIW processors became very popular, particularly for signal processing. Decompression speed is especially important for VLIW architectures given that the length of the instruction word is long. Furthermore, modern VLIW architectures use flexible ...

14 Mixed-signal design and simulation: Symbolic analysis of analog circuits with hard nonlinearity 77%

Alicia Manthe , Zhao Li , C.-J. Richard Shi
Proceedings of the 40th conference on Design automation June 2003

A new methodology is presented to solve a strongly nonlinear circuit, characterized by Piece-Wise Linear (PWL) functions, symbolically and explicitly in terms of its circuit parameters and is amenable to computer implementation. The method is based on a modified nodal formulation of piecewise linear circuit equations as a *mixed* Linear Complementarity Problem (MLCP). The technique of determinant-decision diagrams is applied to implement the symbolic transformation of the MLCP to the standa ...

15 Volume rendering: VIZARD II: a reconfigurable interactive volume rendering system 77%

M. Meißner , U. Kanus , G. Wetekam , J. Hirche , A. Ehlert , W. Straßer , M. Doggett , P. Forthmann , R. Proksa

Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware September 2002

This paper presents a reconfigurable, hardware accelerated, volume rendering system for high quality perspective ray casting. The volume rendering accelerator performs ray casting by calculating the path of the ray through the volume using a programmable Xilinx Virtex FPGA which provides fast design changes and low cost development. Volume datasets are stored on the card in low profile DIMMs with standard connectors allowing both, large datasets up to 1 GByte with 32 bit per voxel, and easy upgr ...

16 Potpourri: A low power direct digital frequency synthesizer with 60 dBc spectral purity 77%

J. M.P. Langlois , D. Al-Khalili

Proceedings of the 12th ACM Great Lakes Symposium on VLSI April 2002

We present a low-power sine-output Direct Digital Frequency Synthesizer (DDFS) realized in 0.18 &mgr;m CMOS that achieves 60 dBc spectral purity from DC to the Nyquist frequency. No ROM or multipliers are used, but an external DAC is required if an analog output is desired. Power consumption is 10 mW for a 100 MHz clock, which is significantly less than figures reported previously. System complexity is greatly reduced by using an efficient linear interpolation scheme to approximate a sinusoid fu ...

17 Structured design implementation: a strategy for implementing regular datapaths on FPGAs 77%

Andreas Koch

Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays February 1996

18 RASP: a general logic synthesis system for SRAM-based FPGAs 77%

Jason Cong , John Peck , Yuzheng Ding

Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays February 1996

19 Logic synthesis for programmable gate arrays 77%

Rajeev Murgai , Yoshihito Nishizaki , Narendra Shenoy , Robert K. Brayton , Alberto Sangiovanni-Vincentelli

Conference proceedings on 27th ACM/IEEE design automation conference January 1991

The problem of combinational logic synthesis is addressed for two interesting and popular classes of programmable gate array architectures: table-look-up and multiplexor-based. The constraints imposed by some of these architectures require new algorithms for minimization of the number of basic blocks of the target architecture, taking into account the wiring resources.

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1 **A radix-2 general division algorithm with carry-free scheme and the divider implementation**
Jen-Shiun Chiang; Hung-Da Chung; Ming-Hsou Tsai;
Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IE International Conference on , Volume: 1 , 5-8 Sept. 1999
Pages:569 - 572 vol.1

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